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10/587,662	07/26/2006	Gerhard Kottschlag	10191/4355	8299

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EXAMINER	
POOS, JOHN W	
ART UNIT	PAPER NUMBER
4125	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/587,662	KOTTSCHLAG, GERHARD	
	Examiner	Art Unit	
	JOHN W. POOS	4125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-14* is/are pending in the application.

4a) Of the above claim(s) *1-7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-11 and 13-14* is/are rejected.

7)☐ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/26/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 8, 11, 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamparian et al. (US 5,990,761).

In regard to Claim 8 (as taught in Figure 5)**:**

A varactor diode alternative circuit, comprising:

at least three varactor diodes that are in each case connected in series alternatingly opposite to one another; and (D1, D2, D3, D4)

at least one of a resistor network and an inductor network, the at least one of the resistor network and the inductor network coupled to the at least three varactor diodes; (50a and 50B connected to D1, D2, and D4)

wherein, at each of the varactor diodes, a control voltage (Vcntl) supplied to the circuit for adjusting capacitance is applied at least approximately at full extent, and an alternating voltage (Vs) that is applied at the series connection of the varactor diodes, which is at a higher frequency compared to the control voltage, (Column 3: lines 25-28 and lines 34-36) is distributed at least approximately uniformly to the varacter diodes. (Vs/4 for D1, D2, D3, D4)

In regard to Claim 11 (as taught in Figure 5)**:**

The varactor diode alternative circuit as recited in claim 8, wherein:

the at least three varactor diodes includes one of an even number of varactor diodes or an even number of parallel connections of varactor diodes; (D1, D2, D3, D4)

at each node of the series connection, respectively either anodes of the diodes or cathodes of the diodes being connected to one another; (D3 and D4 (cathodes) and D2 and D3 (anodes))

the nodes of the anodes lying between the outside terminals being connected via resistors and/or inductors to the anodes of those diodes whose anodes form a first outside terminal and a second outside terminal of the altemative circuit; and (D1 and D4 anodes form the outside terminals)

nodes of the cathodes lying between the outside terminals are connected to at least one of resistors and inductors whose second terminals form the control voltage terminal for supplying the control voltage setting the capacitance. (D1, D2 and D3, D4 cathodes receive the control voltage)

In regard to Claim 13 (as taught in Figure 5)**:**

The varactor diode alternative circuit as recited in claim 8, wherein:

at each node of the series connection, respectively one of anodes of the varactor diodes or cathodes of the varactor diodes are connected to one another; (Figure 5: D3 and D4 (cathodes) and D2 and D3 (anodes))

the anodes are connected to a first additional terminal via at least one of resistors and inductors; and (Figure 5: RFC3)

the cathodes are connected via at least one of resistors and inductors to a second, additional terminal, the first and second additional terminals being used for supplying the control voltage to set the capacitance. (Figure 5: D3 and D4 connected to RFC4 and R2 which is connected to Vcntl)

In regard to Claim 14 (as taught in Figure 5)**:**

An electrical circuit device or an electrical unit, comprising:

a varactor diode alternative circuit including at least three varactor diodes that are in each case connected in series alternatingly opposite to one another; (D1, D2, D3, D4) and at least one of a resistor network and an inductor network, the at least one of the resistor network and the inductor network coupled to the at least three varactor diodes, (50a and 50b) wherein, at each of the varactor diodes, a control voltage (Vcntl) supplied to the circuit for adjusting capacitance is applied at least approximately at full extent, and an alternating voltage (Vs) that is applied at the series connection of the varactor diodes, which is at a higher frequency compared to the control voltage (Column 3: lines 25-28 and lines 34-36), is distributed at least approximately uniformly to the varacter diodes (Vs/4 for D1, D2, D3, D4).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamparian et al. (US 5,990,761), in view of Hasegawa et al. (US 4,536,724).

In regard to Claim 9:

All of the claim limitations are discussed with respect to Claim 8 above except for wherein the at least one of the resistor network and the inductor network is arranged so that anodes of the varactor diodes, with respect to the control voltage supplied to the circuit, are connected to a first electrical potential, and cathodes of the varactor diodes, with respect to the control voltage, are connected to a second electrical potential that is higher, by the control voltage, compared to the first electrical potential.

Hasegawa (724) teaches wherein the at least one of the resistor network and the inductor network is arranged so that anodes of the varactor diodes, with respect to the control voltage

supplied to the circuit, are connected to a first electrical potential, and cathodes of the varactor diodes, with respect to the control voltage, are connected to a second electrical potential that is higher, by the control voltage, compared to the first electrical potential. (Figure 3: where the control input is connected to the cathodes through an inductor and the anodes are connected to ground through an inductor, where it is well known in the art that ground is a low potential)

Therefore it would have been obvious to one skilled in the art at the time of the invention to connect the cathodes to a high potential and the anodes to a low potential in order to have a high carrier-to-noise ratio throughout a wide frequency range (Column 1: lines 59-60).

In regard to Claim 10:

Hamparian (761) teaches at each node of the series connection, respectively either anodes of the varactor diodes or cathodes of the varactor diodes are connected to one another (Figure 5: D1 and D2 (cathodes) and D2 and D3 (anodes)). Hamparian (761) does not teach wherein: nodes of the anodes lying between outside terminals are connected via at least one of resistors and inductors to the anode of a varactor diode whose anode forms a first outside terminal of the alternative circuit; and nodes of the cathodes lying between the outside terminals are connected via at least one of resistors and inductors to the cathode of a varactor diode whose cathode forms a second outside terminal of the circuit.

Hasegawa (724) teaches wherein: the at least three varactor diodes include one of an odd number of varactor diodes or an odd number of parallel connections of varactor diodes (Column 1: lines 61-65); and

nodes of the anodes lying between outside terminals are connected via at least one of resistors and inductors to the anode of a varactor diode whose anode forms a first outside terminal of the alternative circuit; and (Figure 3: 34)

nodes of the cathodes lying between the outside terminals are connected via at least one of resistors and inductors to the cathode of a varactor diode whose cathode forms a second outside terminal of the circuit. (Figure 3: 31)

Therefore it would have been obvious to one skilled in the art at the time of the invention to connect the cathodes to a high potential and the anodes to a low potential in order to have a high carrier-to-noise ratio throughout a wide frequency range (Column 1: lines 59-60).

Allowable Subject Matter

7. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN W. POOS whose telephone number is (571)270-5077. The examiner can normally be reached on M-F (alternating Fridays off), E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. W. P./
Examiner, Art Unit 4125

/Charles D. Garber/
Supervisory Patent Examiner, Art Unit 4125